



# **MALLA REDDY COLLEGE OF ENGINEERING & TECHNOLOGY**

(Sponsored by CMR Educational Society)

(Affiliated to JNTU, Hyderabad, Approved by AICTE - Accredited by NBA & NAAC – 'A' Grade - ISO 9001:2008 Certified)  
Maisammaguda, Dhulapally (Post Via Hakimpet), Secunderabad – 500100

## **DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING**

### **ANALOG & DIGITAL ELECTRONICS MODEL QUESTION PAPERS**

**FOR**

**II B.TECH II SEMESTER  
(R-22)**

**2023-2024**

## EXAM PATTERN

**Time: 3 Hours**

**Max. Marks: 60**

**Note:** This question paper contains two parts A and B.

Part A is compulsory which carries 10 marks. Answer all questions in Part A.

Part B consists of 5 Units. Answer any one full question from each unit. Each question carries 10 marks and may have a, b, c as sub questions.

### UNIT 1

#### PART-A (10Marks)

- 1a) Why transistor is called a current controlling device ?
- b) What is meant by biasing ?
- c) Define stabilization ?
- d) Define operating point ?
- e) State different types of biasing ?
- f) What is meant by AC load line ?
- g) State factors that effect the stability of Q point of a transistor ?
- h) state  $h$  parameters if a transistor
- i) what is meant by DC load line ?
- j) Define  $h$  parameter ?

#### PART-B (50 Marks)

- 2a) Explain about need for biasing of a transistor & state factors affecting stability factor.
  - b) Explain terms bias stabilization and bias compensation
- OR**
- 3a) Compare all the three biasing circuits
  - b) Draw the circuits and explain principles of working of diode compensation for  $V_{be}$  and  $I_{co}$
- 4a) Draw fixed bias circuit and derive expression for stability factor  $S$ .
  - b) Explain AC load line analysis
- OR**
- 5a) Draw self bias circuit and derive expression for stability factor  $S$ .
  - b) Draw & explain  $h$  parameter model in CE configuration
- 6a) Draw Collector to base bias circuit and derive expression for stability factor  $S$ .
  - b) Explain DC load line analysis
- OR**
- 7a) Draw & explain  $h$  parameter model in CB configuration
  - b) state benefits of  $h$  parameters be & why they called so ?
  - 8a) Draw & explain  $h$  parameter model in CC configuration
  - b) Explain process of analysis of CE configuration with simplified hybrid model
- OR**
- 9a) obtain CC  $h$  parameters in terms of CE parameters
  - b) Explain process of analysis of CB configuration with simplified hybrid model

## UNIT 2

### PART-A

(10Marks)

- 1a) Define term "pinchoff" for a FET
- b) What are advantages of FET over BJT ?
- c) State applications of JFET
- d) State types of MOSFET
- e) What are different biasing circuits of FET?
- f) What is meant by gainbandwidth product?
- g) State terminals of a JFET ?
- h) What is purpose of coupling capacitor in CS amplifier ?
- i) State types of FET amplifiers ?
- j) Abbreviate FET

### PART-B

(50 Marks)

- 2a) Explain about JFET Common Source amplifiers
  - b) Compare CS, CD & CG amplifiers
- OR**
- 3a) Explain about JFET Common Drain amplifiers
  - b) Explain hybrid II model of CE transistor model with a neat sketch
- 4a) Compare FET amplifiers performance with BJT amplifiers
  - b) State & explain how FET parameters will be determined ?
- OR**
- 5a) Design FET amplifier
  - b) What is hybrid II model & Derive hybrid II model elements of a CE transistor

## UNIT 3

### PART-A (10Marks)

1. a) Name some positional weighted systems
- b) why is binary number system used in digital system?
- c) What is canonical form ?
- d) How Do You Convert A Decimal Number Into A Number In Any other system with base b?
- e) what is 2's complement method?
- f) What are logic gates & mention all logic gates ?
- g) How BCD addition is performed?
- h) What is POS & SOP?
- i) State basic theorems of Boolean Algebra
- j) How can NOR gate can be used as inverter?

### PART-B (50 Marks)

2. a) Simplify Boolean expression  $Y = (A+B+C+D')(A+B'+C'+D')(A+B+C'+D')(A'+B'+C+D')(A'+B'+C'+D)$
  - b) Verify expression  $x'y' + x'y + xy = x' + y$
- OR**
3. a) Simplify Boolean expression  $Y = ABC' + ABC + A'B'C$  on K-Map
  - b) Verify expression  $(AB+C+D)(C'+D)(C'+D+E) = ABC'+D$
- 4 a) State & Prove Associative law & Distributive law
  - b) Prove NAND Gate as Universal gate [5+5]

**OR**

5. a) Prove NOR gate as Universal gate.
  - b) Develop a gray code for  $(42)_{10}$  and  $(97)_{10}$  and convert them to Hexa sequence
- 6 a) Convert 105.15 to binary
  - b) Convert 11011.101 to decimal
  - c) Convert 163.875 to octal
  - d) convert 756 into hexa decimal

**OR**

- 7.a)convert binary number 1011100010 to grey code
  - b)state steps to convert binary to gray code.
- 8.a) Construct EXNOR & EXOR , OR ,AND by using NAND & NOR gates
  - b)Generate 4 bit gray code using mirror image property

**OR**

- 9.a) a) Convert 378.93 to octal & Convert 5497 to binary [5]
  - b) Convert 1011011011 & 01011111011.011111 to hexadecimal
- 10.a) Represent decimal numbers in Excess-3 code i) 327 ii) 123 iii) 658
  - b) using 2's complement method to subtract i) 01100-00011 ii) 10011-11001

**OR**

- 11.a) perform binary addition in 8-4-2-1 BCD i) 24+18 ii) 48+58
- b) perform  $(1110111000) - (001100010)$  by using 1's complement method

## UNIT 4

### PART-A

(25 Marks)

- 1.a) What is Pair, Quad & Octet in K- Map?
- b) What do you mean by Don't care condition?
- c) what are prime implicants?
- d) State advantages of K-map?
- e) what is maxterm?
- f) what is minterm?

### PART-B

(50 Marks)

2. a) state steps for converting NAND/NOR logic using graphical procedure.
- b) construct Boolean expression  $((A+B)+C) D$  using NOR LOGIC

**OR**

- 3a) simplify given function  $f(w,x,y,z) = \sum(0,1,2,6,7,8,10,12,14,15)$  using k map
- b) Implement function F using two level forms NAND-NAND & OR-NAND  
 $f(A,B,C,D) = \sum m(0,1,4,6,8,9,10,12)$

- 4 a) Define Prime implicants & Essential Prime -Implicants
- b) Implement EX-OR gate using only NAND gates

**OR**

- 5.a) Find prime Implicants and determine which are essential  
 $F(A,B,C,D) = \sum M(0,2,4,5,6,7,8,10,13,15)$
- b) State rules of K-map simplification

6. a) simplify function using K-map  
 $F(A,B,C,D) = M(1,3,4,5,6,11,13,14,15)$

**OR**

- 7.a) state Rules for obtaining NAND/NAND logic diagram.
- b) Implement EX-OR gate using only NOR gates
- 8.a) Reduce function using K map technique  
 $f(A,B,C,D) = \sum m(4,5,7,12,14,15) + d(3,8,10)$
- b) Implement Boolean function with NOR-NOR logic  $Y = AC + BC + AB + D$

- 10.a) Simplify Boolean function  
 $F = A'BC'D + A'BC'D + AB'CD + AB'CD' + ABCD + A'B'CD'$

**OR**

- 11.a) state Rules for obtaining NOR-NOR logic diagram
- b) simplify function & realize using universal gates  
 $F(A,B,C) = A'BC' + ABC + B'C' + A'B'$

**UNIT 5**  
**PART-A(10 Marks)**

- 1.a) What is full Adder?
- b) Explain magnitude comparator
- C) what is comparator ?
- d) why a multiplexer is called a data selector?
- e)What is combinational circuit & sequential circuit?
- f) What is full sub-tractor?
- g)state the difference between flip-flop and latch?
- h)what is encoder ?
- i) Draw excitation table of JK Flip-flop
- j) why is a de-multiplexer is called a distributor ?

**PART-B (50 Marks)**

- 2.a) Draw logic diagram of master slave J K flip- flop using NAND gates and explain it's Truth table
- b) Design 16:1 multiplexer using 8:1 multiplexer

**OR**

- 3.a). Design 2 bit comparator using gates
  - b) state characteristic equation & truth table of SR flip flop along with it's logic diagram
- 4 a)Draw & explain operation of Master-Slave SR flip-flop with block diagram.
  - b) ) Draw & Explain operation of 2's complement adder- subtractor

**OR**

5. a. Explain Race around condition in Flip-flops
  - b) What is Full Adder & Implement Full adder using two half Adders
6. a) Explain characteristic equation of JK Flip-flop from excitation table.
  - b) Draw & explain function of Half - Subtractor & Full -Subtractor with suitable diagrams

**OR**

- 7a). What is Full Adder & Implement Full adder using two half Adders
- b) Design a 5 to 32 decoder using one 2 to 4 and four 3 to 8 decoder ICs

**OR**

- 8a) Design a Full Adder circuit using a 3:8 Decoder
- b) state characteristic equation & truth table of master slave flip flop along with it's logic diagram

- 9a) ) Draw & explain Multiplexer & De-multiplexer
- b) Design octal to binary encoder

- 10a) Draw logic diagram & Truth Table for 4\*2 encoder
- b) Design 16:1 multiplexer using 8:1 multiplexer

**OR**

- 11.a) Design a SR flip flop using AND gates and NOR gates. Explain the operation of the SR flip flop with the help of characteristic table and characteristic equation
- b) ) Design a 4 bit magnitude comparator to compare two 4 bit numbers