MALLAREDDYCOLLEGEOFENGINEERING&TECHNOLOGY

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Maisammaguda, Dhulapally (Post Via Hakimpet), Secunderabad – 500100

DEPARTMENTOFELECTRONICS&COMMUNICATION ENGINEERING

ANALOG&DIGITALELECTRONICS

MODELQUESTIONPAPERS FOR

IIB.TECHIISEMESTER

(R-22)

2024-2025

EXAM PATTERN

Time:3 Hours **Max.Marks:60**

Note: ThisquestionpapercontainstwopartsAandB.
Part Aiscompulsorywhichcarries10marks.Answer allquestionsinPartA.
PartBconsistsof5Units. Answer anyone fullquestionfromeachunit. Eachquestioncarries10 marks and may have a, b, c as sub questions.

UNIT1

PART-A (10Marks)

1a)Whytransistoriscalledacurrentcontrollingdevice?
b) What ismeantbybiasing?
c) Definestabilization?
d) Defineoperatingpoint?
e) Statedifferenttypesofbiasing?
f) what ismeantbyACload line ?
g) Statefactorsthateffectthe stabilityofQ pointofa transistor?
h) statehparametersifatransistor
i) whatismeantbyDCload line ?
j) Definehparameter ?

PART-B (50Marks)

2a)Explainaboutneedfor biasingofatransistor &statefactorsaffectingstabilityfactor.
b)Explaintermsbiasstabilizationandbiascompensation

OR

3a)Compareallthethreebiasingcircuits
b)Drawthecircuitsandexplainprinciplesofworkingofdiodecompensationfor Vbe and Ico

4a)Drawfixedbiascircuitandderiveexpressionfor stabilityfactor S.
b)ExplainACloadlineanalysis

OR

5a)Drawselfbiascircuitandderiveexpressionfor stabilityfactorS.
b)Draw&explainhparametermodelinCE configuration

6a)DrawCollector tobasebiascircuitandderiveexpressionforstabilityfactorS.
b)ExplainDCloadlineanalysis

OR

7a)Draw&explainhparametermodelinCBconfiguration
b) state benefits of h parameters be& why they called so ?
8a)Draw&explainhparameter modelinCCconfiguration
b)ExplainprocessofanalysisofCEconfigurationwithsimplifiedhybridmodel

OR

9a) Compare CC-hparameters with CE parameters
b)ExplainprocessofanalysisofCBconfigurationwithsimplifiedhybridmodel

UNIT2

PART-A (10Marks)

1a)Defineterm"pinchoff"foraFET
b)WhatareadvantageousofFEToverBJT?
c) StateapplicationsofJFET
d)StatetypesofMOSFET
e)what aredifferentbiasingcircuitsofFET?
f)Whatis meantbygainbandwidthproduct?
g)Stateterminalsofa JFET?
h)whatispurposeofcouplingcapacitor inCSamplifier?
i) statetypesofFETamplifiers?
j)Abbrevate FET

PART-B (50Marks)

2a)ExplainaboutJFETCommonSourceamplifiers
b)CompareCS,CD&CG amplifiers

OR

3a)**E**xplainaboutJFETCommonDrainamplifiers
b)ExplainhybridII modelofCEtransistormodelwithaneatsketch

4a)CompareFETamplifiersperformancewithBJT amplifiers
b)State&explainhowFET parameterswillbedetermined?

OR

5a)DesignFET amplifier
b)whatishybridII model&DerivehybridII modelelementsofaCEtransistor

UNIT3

PART-A (10Marks)

1. a)Namesomepositionalweighted systems
   b) whyisbinarynumber systemusedindigitalsystem?
   c) Whatiscanonicalform?
   d) HowDo YouConvertADecimalNumberIntoANumberIn Anyothersystemwithbase b?
   e) whatis2'scomplement method?
   f) Whatarelogicgates&mentionalllogicgates?
   g) HowBCDadditionisperformed?
   h) WhatisPOS&SOP?
   i) State basictheoremsofBooleanAlgebra
   j) How canNOR gatecanbeusedasinverter?

PART-B (50 Marks)

2. a)SimplifyBooleanexpressionY=(A+B+C+D')(A+B'+C'+D')(A+B+C'+D')(A'+B'+C+D') (A'+B'+C'+D)
   b) Verifyexpressionx'y'+x'y+xy=x'+y

OR

3. a)SimplifyBooleanexpressionY=ABC'+ABC+A'B'ConK-Map
   b) Verifyexpression(AB+C+D)(C'+D) (C'+D+E)=ABC'+D

4a) State&ProveAssociativelaw&Distributivelaw
   b)ProveNANDGateasUniversalgate[5+5]

OR

5. a)ProveNORgateasUniversal gate.
   b) Developagraycodefor $(42)_{10}$and$(97)_{10}$andconvertthemtoHexasequence 6 a) Convert 105.15 to binary
   b) Convert11011.101todecimal
   c) Convert163.875to octal
   d) convert756intohexa decimal

OR

7.a)convertbinarynumber 1011100010togreycode
   b)statestepstoconvertbinarytograycode.

8.a)Construct EXNOR&EXOR,OR,ANDbyusingNAND& NOR gates
   b)Generate4bitgraycodeusingmirrorimageproperty

OR

9.a)a)Convert378.93tooctal&Convert5497tobinary[5]
   b)Convert1011011011&01011111011.011111to hexadecimal

10.a)RepresentdecimalnumbersinExcess-3codei)327ii)123iii)658
   b)using2'scomplementmethodtosubtracti)01100-00011ii)10011-11001

OR

perform binary addition in 8-4-2-1 BCDi) 24+18ii) 48+58
   b)perform(1110111000)-(001100010)byusing1'scomplementmethod

UNIT4

PART-A **(25Marks)**

WhatisPair,Quad&OctetinK-Map?

b) WhatdoyoumeanbyDon'tcare condition?

c) whatareprimeimplicants?

d) StateadvantagesofK-map?

e) whatismaxterm?

f) what isminterm?

PART-B **(50 Marks)**

2.a)statestepsforconvertingNAND/NOR logicusinggraphicalprocedure.

b)constructBooleanexpression((A+B)+C)DusingNORLOGIC

OR

3a)simplifygivenfunction **f(w,x,y,z)=∑(0,1,2,6,7,8,10,12,14,15)**usingkmap

b)ImplementfunctionFusingtwolevelformsNAND-NAND&OR-NAND

f(A,B,C,D)=∑m(0,104,6,8,9,10,12)

4a)DefinePrimeimplicants&EssentialPrime-Implicants

b)ImplementEX-ORgateusingonlyNANDgates

OR

5.a)FindprimeImplicantsanddeterminewhichareessential F(A,B,C,D)= ∑ M(0,2,4,5,6,7,8,10,13,15)

b)StaterulesofK-map simplification

6. a) simplify function using K-map

F(A,B,C,D)=M(1,3,4,5,6,11,13,14,15)

OR

7. a)stateRulesforobtainingNAND/NANDlogicdiagram.

b) ImplementEX-ORgateusing onlyNORgates

8. a)Reduce function using K map technique

f(A,B,C,D)=**∑m(4,5,7,12,14,15)+d(3,8,10)**

b) Implement BooleanfunctionwithNOR-NORlogicY=AC+BC+AB+D

10.a) SimplifyBooleanfunction

F=A'BC'D+A'BC'D+AB'CD+AB'CD'+ABCD+A'B'CD'

OR

11.a)stateRulesfor obtainingNOR-NORlogicdiagram

b)simplifyfunction&realizeusinguniversalgates

F(A,B.C)= A'BC' + ABC +B'C" + A'B'

UNIT5

PART-A(10 Marks)

1.a)WhatisfullAdder?
b)Explainmagnitudecomparator
C)whatiscomparator?
d) whyamultiplexeriscalledadataselector?
e) Whatiscombinationalcircuit&sequentialcircuit?
f) What isfullsub-tractor?
g) statethedifferencebetweenflip-flopandlatch?
h) whatisencoder ?
i) DrawexcitationtableofJKFlip-flop
j) whyisade-multiplexeriscalledadistributor?

PART-B(50 Marks)

2.a)DrawlogicdiagramofmasterslaveJKflip- flopusingNANDgatesandexplainit'sTruth table
b)Design16:1multiplexerusing8:1multiplexer

OR

3.a).Design2bitcomparatorusinggates
b)statecharacteristicequation&truthtableofSRflipflopalongwithit'slogic diagram

4a)Draw&explainoperationofMaster-Slave SRflip-flopwithblockdiagram.
b))Draw&Explainoperationof2'scomplementadder- subtractor

OR

5. a.ExplainRacearoundconditioninFlip-flops
b)WhatisFullAdder&ImplementFulladderusingtwohalfAdders

6. a)ExplaincharacteristicequationofJKFlip-flopfromexcitationtable.
b)Draw&explainfunctionofHalf -Subtractor&Full-Subtractorwithsuitablediagrams

OR

7a).WhatisFullAdder&ImplementFulladderusingtwo halfAdders
b)Designa5 to 32decoderusingone2to4andfour3to8decoderICs

OR

8a) DesignaFullAdder circuitusinga3:8Decoder
b)statecharacteristicequation&truthtableofmasterslaveflip flopalongwithit'slogic diagram

9a))Draw&explainMultiplexer &De-multiplexer
b)Designoctaltobinaryencoder

10a) Drawlogicdiagram&TruthTablefor 4*2encoder
b)Design16:1 multiplexerusing8:1multiplexer

OR

11.a)DesignaSRflip flopusing ANDgatesandNORgates.ExplaintheoperationoftheSR flip flop with the help of characteristic table and characteristic equation
b))Designa4bitmagnitudecomparatortocomparetwo4bitnumbers